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Delay Test LOS/LOC) Design Rule Check VLSI -  
Lecture 4: Design Metrics 1-2 Introduction  
Types Of Tests Testing of VLSI Circuits

Design for Testability Test Pattern

Generation The Scope \u0026 Career

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Agrawal. Essentials of Electronic Testing for Digital, Memory, and Mixed-signal VLSI Circuits. New York, NY: Springer, 2000. Syllabus This course examines the theory and practice of fault analysis, test generation, and design for testability for digital circuits and systems.

~~EECS 579 | Electrical & Computer Engineering at Michigan~~

FRONTIERS IN ELECTRONIC TESTING Consulting Editor Vishwani D. Agrawal Books in the series: Analog and Mixed-Signal Boundary-Scan: A Guide to the IEEE 1149.4 Test Standard A. Osseiran ISBN: 0-7923-8686-8

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Instructor: Professor Vishwani D. Agrawal,  
vagrawal@eng.auburn.edu, Brown 323,  
334-844-1853. Text book: Essentials of  
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12: DFT and Scan 4 Scan Design Scan Design  
Circuit is designed using pre-specified  
design rules. Test structure (hardware) is  
added to the verified design: Add a test  
control (TC) primary input. Replace flip-  
flops by scan flip-flops (SFF) and connect to  
form one or more shift registers in the test  
mode. Make input/output of each scan shift  
register controllable/observable from PI/P0.  
Use combinational ATPG to obtain tests for  
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