Accelerate C In Fpga

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Accelerate C In Fpga
Recent advances in C-to-FPGA design methodologies and tools facilitate the rapid creation of hardware-accelerated embedded systems. By Glenn Steiner, Kunal Shenoy, Dan Isaacs (Xilinx), and David ...

How to accelerate algorithms by automatically generating FPGA coprocessors
But when volume doesn't justify an ASIC implementation, FPGAs offer flexible hardware-based alternatives to accelerate complex algorithms. All FPGA suppliers ... (Fig. c). Up to 64 16-bit ...

FPGA Flexibility Lights A Fire Under DSPs
In the clearest confirmation to date that the "C" in "CPU" may soon no longer stand for ... specific or workload-specific acceleration." Intel acquired FPGA accelerator maker Altera in 2015, and gave ...

Intel Shatters Precedent, Embraces Dedicated FPGA Infrastructure Processors
Embedded Supercomputing Embedded computing technology has evolved way past the point now where complete system functionality on single chip is remarkable. To ...

Chip-Level Solutions Feed AI Needs
[Anton] and [Per] are trying to fix that by building his own graphics card around an FPGA. The project is called ... all the work that into this graphics accelerator, it's an amazing piece ...

Open Source Graphics Card
"Silexica's technology complements our existing Vitis solution and roadmap and will accelerate ... Silexica's SLX FPGA tool suite "tackles non-synthesizable and non-hardware aware C/C++ code ...

Programmable chip maker Xilinx acquires C/C++ programming tool provider Silexica
The SLX FPGA tool suite tackles non-synthesisable C/C++ code, non-hardware-aware C/C++ code ... "Silexica's technology complements our existing Vitis solution and roadmap and will accelerate our ...

Xilinx acquires Silexica and its C/C++ tools
Leveraging standard high-level synthesis tools from Xilinx, the SLX FPGA tool suite tackles non-

synthesizable and non-hardware aware C/C++ code ... long-term goal to accelerate the path from ...

Xilinx Acquires Silexica to Broaden its Developer Base
The Cryptographic Coprocessor (or CryptoSoc Accelerator) is a hardware IP core platform that accelerates cryptographic operations in System-on-Chip (SoC) environment on FPGA (Altera SoC ... Siliconch ...

Trng IP Listing
Accelerator RAM with ... Xilinx acquired Silexica, a C/C++ programming and analysis tools company that developed a tool suite for building applications on FPGAs and Adaptive SoCs. Xilinx will ...

Week In Review: Auto, Security, Pervasive Computing
The BittWare IA-Series of FPGA accelerators are designed to help ... Intel's Agilex technology to support three of the most prevalent accelerator form factors used for data center and network ...

BittWare Extends IA-Series of Intel® Agilex™ FPGA-based Accelerator Product Line to Address Data-Intensive Compute, Network and Storage Workloads
The latest addition to the company's Vivado tool suite is believed to be the first FPGA EDA tool suite based on machine ... The EDA design tool enables ML-based algorithms that accelerate design ...

Xilinx adds machine learning optimisation to Vivado to accelerate design cycle
Leveraging standard high-level synthesis tools from Xilinx, the SLX FPGA tool suite tackles non-

synthesizable and non-hardware aware C/C++ code ... long-term goal to accelerate the path from ...

The Globe and Mail
Programmable devices and related technologies provider Xilinx Inc. (XLNX) has acquired Silexca, a privately-held provider of C/C++ programming ... our long-term goal to accelerate the path from ...

Xilinx Snaps up Silexica for Undisclosed Fee
Leveraging standard high-level synthesis tools from Xilinx, the SLX FPGA tool suite tackles non-synthesizable and non-hardware aware C/C++ code, detects application ... is imperative to our long-term ...

This book presents a selection of papers representing current research on using field programmable gate arrays (FPGAs) for realising image processing algorithms. These papers are reprints of papers selected for a Special Issue of the Journal of Imaging on image processing using FPGAs. A diverse range of topics is covered, including parallel soft processors, memory management, image filters, segmentation, clustering, image analysis, and image compression. Applications include traffic sign recognition for autonomous driving, cell detection for histopathology, and video compression. Collectively, they represent the current state-of-the-art on image processing using FPGAs.

FPGA brings high performance applications to market quickly — this book covers the many emerging platforms in a proven, effective manner.

To date, the most common form of simulators of computer systems are software-based running on standard computers. One promising approach to improve simulation performance is to apply hardware, specifically reconfigurable hardware in the form of field programmable gate arrays (FPGAs). This manuscript describes various approaches of using FPGAs to accelerate software-implemented simulation of computer systems and selected simulators that incorporate those techniques. More precisely, we describe a simulation architecture taxonomy that incorporates a simulation architecture specifically designed for FPGA accelerated simulation, survey the state-of-the-art in FPGA-accelerated simulation, and describe in detail selected instances of the described techniques. Table of Contents: Preface / Acknowledgments / Introduction / Simulator Background / Accelerating Computer System Simulators with FPGAs / Simulation Virtualization / Categorizing FPGA-based Simulators / Conclusion / Bibliography / Authors' Biographies

High-Performance Computing using FPGA covers the area of high performance reconfigurable computing (HPRC). This book provides an overview of architectures, tools and applications for High-Performance Reconfigurable Computing (HPRC). FPGAs offer very high I/O bandwidth and fine-grained, custom and flexible parallelism and with the ever-increasing computational needs coupled with the frequency/power wall, the increasing maturity and capabilities of FPGAs, and the advent of multicore processors which has caused the acceptance of parallel computational models. The Part on architectures will introduce different FPGA-based HPC platforms: attached co-processor HPRC architectures such as the CHREC's Novo-G and EPCC's Maxwell systems; tightly coupled HRPC architectures, e.g. the Convey hybrid-core computer; reconfigurably networked HPRC architectures, e.g.

the QPACE system, and standalone HPRC architectures such as EPFL's CONFETTI system. The Part on Tools will focus on high-level programming approaches for HPRC, with chapters on C-to-Gate tools (such as Impulse-C, AutoESL, Handel-C, MORA-C++); Graphical tools (MATLAB-Simulink, NI LabVIEW); Domain-specific languages, languages for heterogeneous computing(for example OpenCL, Microsoft's Kiwi and Alchemy projects). The part on Applications will present case from several application domains where HPRC has been used successfully, such as Bioinformatics and Computational Biology; Financial Computing; Stencil computations; Information retrieval; Lattice QCD; Astrophysics simulations; Weather and climate modeling.

The push to move products to market as quickly and cheaply as possible is fiercer than ever, and accordingly, engineers are always looking for new ways to provide their companies with the edge over the competition. Field-Programmable Gate Arrays (FPGAs), which are faster, denser, and more cost-effective than traditional programmable logic devices (PLDs), are quickly becoming one of the most widespread tools that embedded engineers can utilize in order to gain that needed edge. FPGAs are especially popular for prototyping designs, due to their superior speed and efficiency. This book hones in on that rapid prototyping aspect of FPGA use, showing designers exactly how they can cut time off production cycles and save their companies money drained by costly mistakes, via prototyping designs with FPGAs first. Reading it will take a designer with a basic knowledge of implementing FPGAs to the next-level of FPGA use because unlike broad beginner books on FPGAs, this book presents the required design skills in a focused, practical, example-oriented manner. In-the-trenches expert authors assure the most applicable advice to practicing engineers Dual focus on successfully making critical decisions and avoiding common pitfalls appeals to engineers pressured for speed and perfection

Hardware and software are both covered, in order to address the growing trend toward "cross-pollination" of engineering expertise

This book presents an evaluation methodology to design future FPGA fabrics incorporating hard embedded blocks (HEBs) to accelerate applications. This methodology will be useful for selection of blocks to be embedded into the fabric and for evaluating the performance gain that can be achieved by such an embedding. The authors illustrate the use of their methodology by studying the impact of HEBs on two important bioinformatics applications: protein docking and genome assembly. The book also explains how the respective HEBs are designed and how hardware implementation of the application is done using these HEBs. It shows that significant speedups can be achieved over pure software implementations by using such FPGA-based accelerators. The methodology presented in this book may also be used for designing HEBs for accelerating software implementations in other domains besides bioinformatics. This book will prove useful to students, researchers, and practicing engineers alike.

"Many scientific applications rely on the evaluation of elementary transcendental functions (e.g. $\log{(x)}$, $\frac{1}{x}$, $\sqrt{x}$, e^{x}). Software math libraries are a popular approach for realizing such functions, and frequently use series expansion and/or lookup-table-based (LUT-based) methods. However, software approaches necessarily suffer from the traditional overheads of fetching/decoding instructions, limited cache sizes, and so on. To this end, we present hardware accelerators for such functions that deliver high computational throughput, high accuracy and a small circuit. We implement the reciprocal ($\frac{1}{x}$) and square root ($\sqrt{x}$) functions into pipelined hardware accelerators on FPGA. The proposed accelerators are designed with iterative, and

LUT-based algorithms. Here, the LUT-based algorithm uses approximately 1 KB LUT along with a degree-2 polynomial interpolation. All algorithms are specified using C language, and synthesized into RTL with the LegUp HLS~\cite{leguplegup}. In an experimental study, we compare our LUT-based accelerators with IP cores from the Intel/Altera FPGA vendor. Results show that our LUT-based accelerators offer considerably better area usage, while Intel/Altera IP cores operate at a modestly higher throughput. Both ours and Intel/Altera IP cores achieve 1 ULP error. The LUT-based algorithm is generic in the sense that it could be used to implement an entire library of single-precision elementary functions into high-performance hardware accelerators.We also implement a 32-bit integer RISC-V~\cite{riscv} multi-cycle processor on FPGA, which consists of 39 user instructions. The processor is specified using C language, and synthesized into RTL with the LegUp HLS~\cite{leguplegup}. Custom testing programs are developed to verify if each instruction adheres to the RISC-V specification. We demonstrate that through changes to the \texttt{C} specification and HLS constraints, RISC-V processors with different performance/area trade-offs can be explored rapidly. One implementation of the multi-cycle processor uses 795 ALMs (adaptive logic modules) on an Intel/Altera Cyclone V FPGA, and is operable at 124.1 MHz. We believe that, in the future, integrating high-performance elementary transcendental function accelerators into a RISC-V soft processor on FPGAs may bring significant performance benefits to accelerate compute-intensive applications"--

This book summarizes the key scientific outcomes of the Horizon 2020 research project TULIPP: Towards Ubiquitous Low-power Image Processing Platforms. The main focus lies on the development of high-performance, energy-efficient embedded systems for the growing range of increasingly complex image processing applications. The holistic TULIPP approach is described in the book, which addresses

hardware platforms, programming tools and embedded operating systems. Several of the results are available as open-source hardware/software for the community. The results are evaluated with several use cases taken from real-world applications in key domains such as Unmanned Aerial Vehicles (UAVs), robotics, space and medicine. Discusses the development of high-performance, energy-efficient embedded systems for the growing range of increasingly complex image processing applications; Covers the hardware architecture of embedded image processing systems, novel methods, tools and libraries for programming those systems as well as embedded operating systems to manage those systems; Demonstrates results with several challenging applications, such as medical systems, robotics, drones and automotive.

This book makes powerful Field Programmable Gate Array (FPGA) and reconfigurable technology accessible to software engineers by covering different state-of-the-art high-level synthesis approaches (e.g., OpenCL and several C-to-gates compilers). It introduces FPGA technology, its programming model, and how various applications can be implemented on FPGAs without going through low-level hardware design phases. Readers will get a realistic sense for problems that are suited for FPGAs and how to implement them from a software designer's point of view. The authors demonstrate that FPGAs and their programming model reflect the needs of stream processing problems much better than traditional CPU or GPU architectures, making them well-suited for a wide variety of systems, from embedded systems performing sensor processing to large setups for Big Data number crunching. This book serves as an invaluable tool for software designers and FPGA design engineers who are interested in high design productivity through behavioural synthesis, domain-specific compilation, and FPGA overlays. Introduces FPGA technology to software developers by giving an overview of FPGA

programming models and design tools, as well as various application examples; Provides a holistic analysis of the topic and enables developers to tackle the architectural needs for Big Data processing with FPGAs; Explains the reasons for the energy efficiency and performance benefits of FPGA processing; Provides a user-oriented approach and a sense for where and how to apply FPGA technology.

Embedded Systems Design with Platform FPGAs introduces professional engineers and students alike to system development using Platform FPGAs. The focus is on embedded systems but it also serves as a general guide to building custom computing systems. The text describes the fundamental technology in terms of hardware, software, and a set of principles to guide the development of Platform FPGA systems. The goal is to show how to systematically and creatively apply these principles to the construction of application-specific embedded system architectures. There is a strong focus on using free and open source software to increase productivity. Each chapter is organized into two parts. The white pages describe concepts, principles, and general knowledge. The gray pages provide a technical rendition of the main issues of the chapter and show the concepts applied in practice. This includes step-by-step details for a specific development board and tool chain so that the reader can carry out the same steps on their own. Rather than try to demonstrate the concepts on a broad set of tools and boards, the text uses a single set of tools (Xilinx Platform Studio, Linux, and GNU) throughout and uses a single developer board (Xilinx ML-510) for the examples. Explains how to use the Platform FPGA to meet complex design requirements and improve product performance Presents both fundamental concepts together with pragmatic, step-by-step instructions for building a system on a Platform FPGA Includes detailed case studies, extended real-world examples, and lab exercises